

## SERIAL BUS SYSTEM

5 The present application hereby claims priority under 35 U.S.C. § 119 on German Patent Application No. 10008081.2, filed February 22, 2000, the entire contents of which are hereby incorporated herein by reference for all purposes.

### Field of the Invention

10 The present invention relates to a serial bus system having a bus master and at least one bus slave which are connected to one another via at least one bus line. In particular, it relates to a bus system in accordance with the AS-i specification,

- 15 - with the bus system being operable in a normal mode in which, at the latest after a normal cycle time has elapsed, the bus master transmits digital signals to the at least one bus slave, and the at least one bus slave transmits digital signals back to the bus master after each such transmission,
- 20 - with each of the transmitted digital signals being interpreted as a logic zero when a first predetermined current waveform is applied to the bus line,
- with each of the transmitted digital signals being interpreted as a logic one when a second predetermined current waveform, which is different to the first predetermined current waveform, is applied to  
25 the bus line.

### Background of the Invention

Such a bus system (the AS-i bus system in accordance with EN 50 295 is a typical example of this) is highly resistant to interference and defects. It is thus widely used for rugged industrial purposes. As a rule,  
30 such a bus system is supplied from an electrical main system via intermediate power supply devices.

In contrast, different bus systems are generally used for battery power. This applies in particular to systems which need to be able to react to external influences at any time. This is because, in the bus system of  
35 this generic type, a data transfer is always required, which would excessively quickly exhaust a battery owing to the comparatively high power load. The bus systems used for battery power can be operated in a

manner which is resistant to interference and defects only with considerable complexity in comparison to the AS-i bus.

### Summary of the Invention

5 The object of the present invention is to provide a bus system which, firstly, has low power consumption so that it can also be used for battery power, and which can nevertheless be operated easily in a manner which is resistant to interference and defects.

10 The object is achieved in that the bus system of this generic type is developed further such that it can also be operated in an energy saving mode in which the bus master does not transmit any digital signals to the at least one bus slave within the normal cycle time.

15 It is possible that, in the energy saving mode and at the latest after any energy saving cycle time has elapsed, which is longer than the normal cycle time, the bus master transmits digital signals to the at least one bus slave. The at least one bus slave then transmits digital signals back to the bus master after each such transmission. If required, such an energy saving mode may even have a number of energy saving stages. However, it is even better if the bus master no longer transmits any digital signals to the at least one bus slave in the energy saving mode.

20 Switching back to the normal mode is particularly simple if, in the energy saving mode, at least one bus slave monitors the bus line for the application of the first and/or of the second predetermined current waveform and switches back to the normal mode on detection of the application of the first and/or of the second predetermined current waveform.

25 If, at least in the energy saving mode, the first and/or second predetermined current waveform can be applied automatically to the bus line by the at least one bus slave, if, in the energy saving mode, the bus master monitors the bus line for the application of the first and/or of the second predetermined current waveform, and if the bus master switches back to the normal mode on detection of the application of the first and/or of the second predetermined current waveform, the process of switching back to the normal mode can also be initiated by the bus slave. In particular, this allows continuous monitoring for external input signals.

35 The bus master can transmit a switching signal to the at least one bus slave in order to switch to the energy saving mode. Alternatively, the at least one bus slave can monitor for the end of the normal cycle time, and

can switch to the energy saving mode automatically when the normal cycle time elapses.

5 If a predetermined zero current level is applied to the bus line in order to apply the first predetermined current waveform during a zero time, and a predetermined one current level is applied to the bus line in order to apply the second predetermined current waveform during a one time which is different to the zero time the production of two mutually different current waveforms can be achieved easily in terms of circuitry.

10 If there is a current pause between the application of the zero current level and the application of the one current level, data transmission is even more resistant to interference and defects.

If the zero current level is equal to the one current level, this further simplifies the circuitry implementation.

15 The problems resulting from battery supply are particularly applicable in motor vehicles which are intended to be parked for lengthy periods. This is because, in the case of modern motor vehicles, the burglar alarm system and the central locking system, in particular, must be operated all the time while, on the other hand, the automobile battery must not be discharged even after several weeks.

## 20 BRIEF DESCRIPTION OF THE DRAWINGS

Further advantages and details result from the following description of an exemplary embodiment and drawings in which, illustrated in principle:

Figure 1 shows a serial bus system,

Figure 2 shows a bus module, and

25 Figure 3 shows data transmission.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENT

30 According to Figure 1, a bus system has a bus master 1 and bus slaves 2. In this case, there are three bus slaves 2 in the exemplary embodiment. However, in principle, a greater or lesser number of bus slaves 2 could also be connected to the bus master 1.

35 The bus modules 1, 2, that is to say the bus master 1 and the bus slaves 2, are supplied with electrical power via a power supply unit 3 with downstream inductors 4 and power supply lines 7 from a 12 V automobile battery in a passenger-carrying vehicle, for example. The bus master 1 is connected to further bus systems via a vehicle bus 5, for example a CAN bus. The further bus systems are not illustrated in Figure 1, for the sake of

brevity and clarity. These may be constructed in the same way as, or else differently from, the bus system illustrated in Figure 1. The bus slaves 2 detect input signals from a unit 6 in the motor vehicle, for example from a vehicle door, or emit output signals to this unit 6. The bus system is thus  
5 used to control the unit 6 in the motor vehicle, for example, as already mentioned, a door module.

According to Figure 1, the bus modules 1, 2 are also connected to one another for data transmission purposes via the power supply lines 7. The bus system is in consequence in the form of a serial bus system. If  
10 required, one of the power supply lines 7 could even be dispensed with and replaced by a ground connection. According to the exemplary embodiment, the bus system is preferably a bus system in accordance with the AS-i specification.

In normal operation, the bus master 1 cyclically and successively  
15 transmits digital signals to each of the bus slaves 2. After each such transmission, the addressed bus slave 2 then likewise transmits digital signals back to the bus master 1. The cyclic data transmission and the maximum bus extent (.. bus slaves 2), which is predetermined on a system-specific basis, thus ensure that each bus slave 2 receives digital  
20 signals transmitted from the bus master 1, and transmits digital signals back to the bus master 1, at the latest after a normal cycle time has elapsed. The type of data transmission will in this case be explained in more detail in the following text in conjunction with Figures 2 and 3.

According to Figure 2, each of the bus modules 1, 2 bridges the  
25 power supply lines 7 with a high-value resistor 8 and a switching element 9, in addition to a current limiting resistor 9 connected upstream or downstream thereof. Furthermore, the power supply lines 7 are connected to a control circuit 10 for the respective bus module 1, 2. The resistor 8 is chosen to be sufficiently large that the loss current flowing via the resistor 8  
30 is negligibly small. The resistor 8 is used only to detect the potential difference between the power supply lines 7.

According to Figure 3, for data transmission of a one signal, the  
switching element 9 is actuated by the control circuit 10 during a one time T1 so that current with a current level I0 flows through the switching  
35 element 9 and thus into the power supply lines 7 during the one time T1. In order to transmit a digital zero, the switching element 9 is likewise actuated in such a manner that the current level I0 flows, but this time during a zero time T0. The times T0, T1 are different from one another. Furthermore,

they are separated by a current pause  $\Delta T$ . These two mutually different waveforms allow a logic zero and a logic one to be distinguished from one another.

5 An operating voltage  $U_0$  is generally dropped across the power supply lines 7. Owing to the inductors 4, voltage pulses  $P$  are superimposed on this operating voltage  $U_0$ , due to the current waveforms. The voltage pulses  $P$  are detected by the other bus modules 1, 2 via their resistors 8. The interval between two voltage pulses  $P$  makes it possible to detect whether the digital signal being transmitted must be interpreted as a  
10 logic zero or as a logic one.

To the extent described so far, the bus system as shown in Figures 1 to 3 complies with the AS-i protocol. In this case and in accordance with EN 50 295, the normal cycle time is 5 ms.

15 However, according to the invention, the bus system can also be operated in an energy saving mode. In this energy saving mode, the bus master 1 either transmits no digital signals at all to the bus slaves 2, or else transmits digital signals only at considerably longer time intervals than is otherwise the case. The bus master 1 therefore does not necessarily transmit any digital signals to the bus slaves 2 within the normal cycle time.

20 For example, it is possible for the bus master 1 to transmit a switching signal to the bus slaves 2, and for the bus slaves 2 then to switch to the energy saving mode. After this, the bus master 1 completely ceases any further transmission of digital signals. The bus slaves 2 then monitor the power supply lines 7 just for the current pulses  $P$ , which corresponds to the application of one of the digital signals. When they detect such a digital  
25 signal, they switch back to the normal mode.

According to the AS-i Standard EN 50 295, the bus slaves 2 cannot initiate data transmission. They can only react to a data transmission from the bus master 1. Thus, according to the AS-i standard, the bus slaves 2  
30 cannot automatically apply a current waveform with the current level  $I_0$  to the power supply lines 7. If, when it is in the energy saving mode, the bus master 1 also monitors the power supply lines 7 for the application of a current with a current level  $I_0$  - or, corresponding to this, for the occurrence of the voltage pulses  $P$  - and switches back to the normal mode on  
35 detection of these voltage pulses  $P$ , then it is also possible to allow such automatic application of the current waveform by the bus slave 2. This makes sense in particular when the bus system "wakes itself up" on the basis of a state change of the controlled unit 6.

In a passenger-carrying vehicle, for example, each door module may have its own associated bus system of the type illustrated in Figure 1. Each bus system automatically controls and monitors its associated door module. The individual bus systems for the door modules (normally two to  
5 five for a passenger-carrying vehicle) are connected to one another via the vehicle bus 5. If, for example, a vehicle door is now unlocked, the bus slave 2 which is monitoring this door lock registers the fact that the door lock has been unlocked. It thus transmits an appropriate message to the bus master 1. The bus master 1 then in turn transmits digital signals to the other bus  
10 slaves 2, so that, for example, the electric window winder is also activated. Furthermore, the bus master 1 transmits a message via the vehicle bus 5 to the bus masters of the other bus systems that "its" door has been unlocked. On the basis of the "central locking system" functionality, these bus masters now "wake up" their bus systems, so that the other door locks  
15 are also unlocked. Normally, the vehicle is started shortly after this. The vehicle generator in consequence produces electrical power so that the battery is not drained by the bus systems continuing to remain in the normal mode.

According to the exemplary embodiment, the bus slaves 2 switch to  
20 the energy saving mode on the basis of an appropriate control command being transmitted by the bus master 1. However, alternatively, it would also be possible for the bus slaves 2 to monitor for the end of the normal cycle time, and to switch themselves to the energy saving mode automatically when this time elapses.

Furthermore, according to the exemplary embodiment, data  
25 transmission via the power supply lines 7 ceases completely in the energy saving mode. Alternatively, it would also be possible for the data transmissions to be continued at a lower sampling rate. The sampling rate can in this case, if required, be reduced in a number of steps. In this  
30 situation, the bus master 1 transmits digital signals to the bus slaves 2 in the energy saving mode at the latest after an energy saving cycle time which is longer than the normal cycle time has elapsed. These bus slaves 2 respond - as in the normal mode - by transmitting digital signals back to the bus master 1.

35 The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such

modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.